In the Claims:

Please cancel claims 17-21. Please amend claims 1, 4, 5, and 10. Please add new claims 22-34. The claims are as follows:

1. (Currently Amended) A method for forming a transistor, the method comprising the steps of:

a) providing a semiconductor substrate;

b) ~~providing~~ forming an epitaxial layer on [[a]] the substrate;

b) ~~providing~~ forming a dopant source layer on the epitaxial layer; and

c) diffusing dopant from the dopant source layer into the epitaxial layer~~, said dopant diffusion forming~~ to form at least a portion of an extrinsic base for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the extrinsic base being disposed between the dopant source layer and an intrinsic base for the transistor, said intrinsic base being totally within the epitaxial layer.

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2. (Original) The method of claim 1 wherein the dopant source layer comprises a doped single crystal layer formed on the epitaxial layer.

3. (Original) The method of claim 2 wherein the dopant source layer is doped between $5x10^{19}$ and $1x10^{21}$ atoms/cm^3.

4. (Currently Amended) The method of claim 1 further comprising the step of implanting into the epitaxial layer, the implanting forming a second portion of the extrinsic base for the transistor.

5. (Currently Amended) The method of claim 1 further comprising the step of forming a pedestal on the epitaxial layer, and wherein the dopant source layer is formed around the pedestal such that the pedestal defines a portion of the epitaxial layer in which the dopant source layer is not formed on the epitaxial layer.

6. (Original) The method of claim 5 wherein the pedestal further defines an emitter opening.

7. (Original) The method of claim 5 wherein the step of forming a pedestal comprises forming a high pressure oxide layer, a nitride layer, and an oxide layer, and patterning the high pressure oxide layer, nitride layer and oxide layer.

8. (Original) The method of claim 5 wherein the step of forming a pedestal comprises depositing and patterning an oxide layer.'

9. (Original) The method of claim 1 wherein the dopant source layer comprises a raised portion of the extrinsic base.

10. (Currently Amended) A method for forming bipolar transistor on a semiconductor substrate, the method comprising the steps of:

a) providing a semiconductor substrate;

b) forming an epitaxial layer on the semiconductor substrate;

c) forming a pedestal on the epitaxial layer, the pedestal defining an emitter region of the epitaxial layer;

d) forming a dopant source layer on the epitaxial layer, the dopant source layer not formed on the epitaxial layer where the pedestal is on the epitaxial layer; and

e) diffusing dopant from the dopant source layer ~~and~~ into the epitaxial layer to form at least a portion of an extrinsic base for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the extrinsic base being disposed between the dopant source layer and an intrinsic base for the transistor, said intrinsic base being totally within the epitaxial layer.

11. (Original) The method of claim 10 wherein the epitaxial layer comprises silicon germanium.

12. (Original) The method of claim 10 wherein the step of forming a pedestal comprises forming a high pressure oxide layer, a nitride layer, and an oxide layer, and patterning the high pressure oxide layer, nitride layer and oxide layer.

13. (Original) The method of claim 10 wherein the step of forming a pedestal comprises depositing and patterning an oxide layer.

14. (Original) The method of claim 10 wherein the dopant source layer comprises a raised portion of the extrinsic base.

15. (Original) The method of claim 10 further comprising the step of implanting into epitaxial layer, the implanting forming a second portion of the extrinsic base for the transistor.

16. (Original) The method of claim 10 wherein the dopant source layer is self-aligned to the pedestal.

17-21. (Canceled)

22. (New) A method for forming a transistor, the method comprising the steps of:

providing a semiconductor substrate;

forming an epitaxial layer on the substrate;

forming a dopant source layer on a first portion of the epitaxial layer;

forming an emitter material on a second portion of the epitaxial layer, said second portion of the epitaxial layer being adjacent to said first portion of the epitaxial layer;

diffusing dopant from the dopant source layer into the epitaxial layer to form at least a portion of an extrinsic base for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the extrinsic base being disposed between the dopant source layer and an intrinsic base for the transistor, said intrinsic base being totally within the epitaxial layer; and

diffusing emitter dopant from the emitter material into said second portion of the epitaxial layer, said emitter dopant diffusion forming an emitter for the transistor, said emitter being totally within the epitaxial layer, said emitter being surrounded by said portion of the extrinsic base.

23. (New) The method of claim 22, wherein the step of diffusing emitter dopant from the emitter material is performed concurrent with the step of diffusing dopant from the dopant source layer.

24. (New) The method of claim 23, wherein the step of diffusing emitter dopant from the emitter material and the step of diffusing dopant from the dopant source layer are performed by an annealing process.

25. (New) The method of claim 22, said method further comprising the steps of:

providing a cap layer on the dopant source layer; and

providing a spacer layer on the cap layer,

wherein a first surface of the spacer layer is in direct mechanical contact with a surface of the emitter material,

wherein a second surface of the spacer layer is in direct mechanical contact with a first surface of the cap layer,

wherein a second surface of the cap layer is in direct mechanical contact with a surface of the dopant source layer, and

wherein the surface of the emitter material, the first surface of the spacer layer, the second surface of the spacer layer, the first surface of the cap layer, the second surface of the cap layer, and the surface of the dopant source layer are about parallel comprising the steps of:

26. (New) The method of claim 22, said method further comprising the steps of:

forming a subcollector within the semiconductor substrate; and

forming a pedestal implant within the semiconductor substrate, wherein the pedestal implant has a first surface and an opposing second surface, wherein the first surface of the pedestal implant is in direct mechanical contact with the subcollector, wherein the second surface of the pedestal implant is in direct mechanical contact with the intrinsic base, and wherein the pedestal implant is not in direct mechanical contact with said portion of the extrinsic base.

27. (New) The method of claim 26, wherein the step of forming the subcollector is performed before the step of forming the pedestal implant.

28. (New) The method of claim 26, said method further comprising the step of: forming deep trench isolation at the edges of the subcollector, said deep trench isolation surrounding the subcollector and electrically isolating the subcollector.

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29. (New) The method of claim 1, said method further comprising the steps of:

forming a subcollector within the semiconductor substrate; and

forming a pedestal implant within the semiconductor substrate, wherein the pedestal implant has a first surface and an opposing second surface, wherein the first surface of the pedestal implant is in direct mechanical contact with the subcollector, wherein the second surface of the pedestal implant is in direct mechanical contact with the intrinsic base, and wherein the pedestal implant is not in direct mechanical contact with said portion of the extrinsic base.

30. (New) The method of claim 29, wherein the step of forming the subcollector is performed

before the step of forming the pedestal implant.

31. (New) The method of claim 29, said method further comprising the step of: forming deep trench isolation at the edges of the subcollector, said deep trench isolation surrounding the subcollector and electrically isolating the subcollector.

32. (New) The method of claim 10, said method further comprising the steps of:

forming a subcollector within the semiconductor substrate; and

forming a pedestal implant within the semiconductor substrate, wherein the pedestal implant has a first surface and an opposing second surface, wherein the first surface of the pedestal implant is in direct mechanical contact with the subcollector, wherein the second surface of the pedestal implant is in direct mechanical contact with the intrinsic base, and wherein the pedestal implant is not in direct mechanical contact with said portion of the extrinsic base.

33. (New) The method of claim 32, wherein the step of forming the subcollector is performed before the step of forming the pedestal implant.

34. (New) The method of claim 32, said method further comprising the step of: forming deep trench isolation at the edges of the subcollector, said deep trench isolation surrounding the subcollector and electrically isolating the subcollector.